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Jurgen Vollrath			PRENTY, MARK V	
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			2822	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Paper No(s)/Mail Date

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)

5) Notice of Informal Patent Application (PTO-152)

6) Other:

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This Office Action is in response to the papers filed on November 17, 2003.

The drawings filed on November 17, 2003 are informal. Formal replacement drawings are required in response to this Office Action. Note that what appears to be Fig. 2 incorrectly contains a "Figure 1" label inside the box. Correction is required.

Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Widmann et al. (United States Patent 6,404,034 – hereafter Widmann).

With respect to independent claim 1, Widmann discloses a MOS transistor with reduced drain capacitance (see the entire patent, including the Fig. 1 disclosure) comprising a drain 5/8, and a lateral isolation trench 3 extending at least partially underneath the drain.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Widmann.

With respect to dependent claim 3, Widmann's trench is filled with an insulator 4.

Claim 3 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Widmann.

With respect to dependent claim 4, Widmann's insulator 4 is a high step coverable insulating material (note Widmann's claim 5).

Claim 4 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Widmann.

Claims 1, 3, 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawakita et al. (United States Patent 4,685,198 – hereafter Kawakita).

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With respect to independent claim 1, Kawakita discloses a MOS transistor with reduced drain capacitance (see the entire patent, including the Fig. 2 disclosure) comprising a drain 52 (or 56), and a lateral isolation trench 40 extending at least partially underneath the drain.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kawakita.

With respect to dependent claim 3, Kawakita's trench is filled with an insulator 42.

Claim 3 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kawakita.

With respect to independent claim 8, Kawakita discloses a method of forming a laterally extending trench in a semiconductor material underneath a drain of a MOS transistor (see the entire patent, including the Fig. 2 disclosure), comprising choosing a predetermined crystal orientation (see column 4, lines 27-29), etching a vertically extending STI region 28 next to (what will be) the drain 52 (or 56), and using an anisotropic etchant to etch a trench 40 extending laterally from the STI (see column 5, lines 3-8).

Claim 8 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kawakita.

With respect to dependent claim 9, Kawakita's choosing the crystal orientation includes choosing a wafer with a <100> orientation (see column 4, lines 27-29).

Claim 9 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kawakita.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimbo et al. (United States Patent 4,638,552 – hereafter Shimbo).

With respect to independent claim 1, Shimbo discloses a MOS transistor with reduced drain capacitance (see the entire patent, including the Fig. 7 disclosure) comprising a drain 80, and a lateral isolation trench 72 extending at least partially underneath the drain.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Shimbo.

With respect to dependent claim 2, Shimbo's trench 72 is filled with air.

Claim 2 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Shimbo.

Claims 5-7 and 10-15 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose the allowable MOS transistor with reduced drain capacitance taken as a whole, including the lateral isolation trench.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark V. Prenty Primary Examiner

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